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METHODS OF SELECTIVE DEPOSITION OF HEAVILY DOPED EPITAXIAL SiGe

INVENTORS:

YIHWAN KIM

ARKADII V. SAMOILOV

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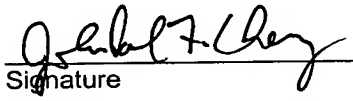
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METHODS OF SELECTIVE DEPOSITION OF HEAVILY DOPED EPITAXIAL SiGe

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] Embodiments of the invention generally relate to the field of semiconductor manufacturing processes and devices, more particular, to methods of depositing silicon-containing films forming semiconductor devices.

Description of the Related Art

[0002] As smaller transistors are manufactured, ultra shallow source/drain junctions are becoming more challenging to produce. According to the International Technology Roadmap for Semiconductors (ITRS), junction depth is required to be less than 30 nm for sub-100 nm CMOS (complementary metal-oxide semiconductor) devices. Conventional doping by implantation and annealing is less effective as the junction depth approaches 10 nm. Doping by implantation requires a post-annealing process in order to activate dopants and post-annealing causes enhanced dopant diffusion into layers.

[0003] Recently, heavily-doped (about $>10^{19}$ atoms/cm^3), selective SiGe epitaxy has become a useful material to deposit during formation of elevated source/drain and source/drain extension features. Source/drain extension features are manufactured by etching silicon to make a recessed source/drain feature and subsequently filling the etched surface with a selectively grown SiGe epilayer. Selective epitaxy permits near complete dopant activation with *in-situ* doping, so that the post annealing process is omitted. Therefore, junction depth can be defined accurately by silicon etching and selective epitaxy. On the other hand, the ultra shallow source/drain junction inevitably results in increased series resistance. Also, junction consumption during silicide formation increases the series resistance even further. In order to compensate for junction consumption, an elevated source/drain is epitaxially and selectively grown on the junction.

[0004] Selective Si epitaxial deposition and SiGe epitaxial deposition permits growth of epilayers on Si moats with no growth on dielectric areas. Selective epitaxy can be used in semiconductor devices, such as within elevated source/drains, source/drain extensions, contact plugs, and base layer deposition of bipolar devices. Generally, a selective epitaxy process involves two reactions: deposition and etching. They occur simultaneously with relatively different reaction rates on Si and on dielectric surface. A selective process window results in deposition only on Si surfaces by changing the concentration of an etchant gas (*e.g.,* HCl). A popular process to perform selective, epitaxy deposition is to use dichlorosilane (SiH_2Cl_2) as a silicon source, germane (GeH_4) as a germanium source, HCl as an etchant to provide selectivity during the deposition and hydrogen (H_2) as a carrier gas.

[0005] Although SiGe epitaxial deposition is suitable for small dimensions, this approach does not readily prepare doped SiGe, since the dopants react with HCl. The process development of heavily boron doped (*e.g.,* higher than 5×10^{19} cm^{-3}) selective SiGe epitaxy is a much more complicated task because boron doping makes the process window for selective deposition narrow. Generally, when more boron concentration (*e.g.,* B_2H_6) is added to the flow, a higher HCl concentration is necessary to achieve selectivity due to the increase growth rate of deposited film(s) on any dielectric areas. This higher HCl flow rate proportionally reduces boron incorporation into the epilayers presumably because the B-Cl bond is stronger than Ge-Cl and Si-Cl bonds.

[0006] Therefore, there is a need to have a process for selectively and epitaxially depositing silicon and silicon compounds with an enriched dopant concentration. Furthermore, the process must maintain a high growth of the deposited material. Also, the process must have less dependency on germanium and boron concentrations in the silicon compound in relation to an etchant flow rate.

SUMMARY OF THE INVENTION

[0007] In one embodiment, the invention generally provides a method of depositing a silicon germanium film on a substrate comprising placing the substrate

within a process chamber and heating the substrate surface to a temperature in a range from about 500°C to about 900°C while maintaining a pressure in a range from about 0.1 Torr to about 200 Torr. A deposition gas is provided to the process chamber and includes SiH_4, GeH_4, HCl, a carrier gas and at least one dopant gas, such as diborane, arsine or phosphine. A doped silicon germanium film is epitaxially grown on the substrate.

[0008] In another embodiment, the invention generally provides a selective epitaxial method for growing a doped silicon germanium film on a substrate comprising placing the substrate within a process chamber at a pressure in a range from about 0.1 Torr to about 200 Torr and heating the substrate surface to a temperature in a range from about 500°C to about 900°C. A deposition gas is provided to the process chamber and includes SiH_4, a germanium source, an etchant source, a carrier gas and at least one dopant gas. The silicon germanium film is grown with a dopant concentration in a range from about 1×10^{20} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3.

[0009] In another embodiment, the invention generally provides a selective epitaxial method for growing a silicon-containing film on a substrate comprising placing the substrate within a process chamber at a pressure in a range from about 0.1 Torr to about 200 Torr and heating the substrate surface to a temperature in a range from about 500°C to about 900°C. A deposition gas is provided to the process chamber and includes SiH_4, HCl and a carrier. The silicon-containing film is grown at a rate between about 50 Å/min and about 600 Å/min.

[0010] In another embodiment, the invention generally provides a selective epitaxial method for growing a silicon-containing film on a substrate comprising placing the substrate within a process chamber at a pressure in a range from about 0.1 Torr to about 200 Torr, heating the substrate to a temperature in a range from about 500°C to about 900°C, providing a deposition gas comprising Cl_2SiH_2, HCl and a carrier gas and depositing a silicon-containing layer on the substrate. The method further comprises providing a second deposition gas comprising SiH_4, HCl

and a second carrier gas and depositing a second silicon-containing layer on the silicon-containing layer.

[0011] In another embodiment, the invention generally provides a method of selectively depositing a silicon-containing film on a substrate comprising placing the substrate within a process chamber, heating the substrate to a temperature in a range from about 500°C to about 900°C and maintaining a pressure in a range from about 0.1 Torr to about 200 Torr. The method further comprises providing a deposition gas comprising a silicon-containing gas, a germanium source, HCl, at least one dopant gas and a carrier gas selected from the group consisting of N_2, Ar, He and combinations thereof and depositing the silicon-containing film epitaxially on the substrate

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0013] Figures 1A-C show several devices with epitaxially deposited silicon-containing layer; and

[0014] Figures 2A-F show schematic illustrations of fabrication techniques for a source/drain extension device within a MOSFET.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0015] The invention provides a process to epitaxially deposit silicon containing compounds during the manufacture of various device structures. In some embodiments, the process utilizes the silicon precursor silane (SiH_4) during the

deposition of silicon compounds. While past techniques usually have used silicon precursors such as dichlorosilane, tetrachlorosilane or hexachlorodisilane, processes of the present invention teach the utilization of silane as a precursor. The use of silane has been found to deposit silicon containing films more quickly than that of dichlorosilane. Also, the use of silane during these processes provides a higher degree of control for dopant concentrations within the film and increased deposition rate.

[0016] Embodiments of the present invention teach processes to grow films of selective, epitaxial silicon compounds. Selective silicon containing film growth generally is conducted when the substrate or surface includes more than one material, such as exposed single crystalline silicon surface areas and features that are covered with dielectric material, such as oxide or nitride layers. Usually, these features are dielectric material. Selective epitaxial growth to the crystalline, silicon surface is achieved while the feature is left bare, generally, with the utilization of an etchant (*e.g.,* HCl). The etchant removes amorphous silicon or polysilicon growth from features quicker than the etchant removes crystalline silicon growth from the substrate, thus selective epitaxial growth is achieved.

[0017] Carrier gases are used throughout the processes and include H_2, Ar, N_2, He and combinations thereof. In one example, H_2 is used as a carrier gas. In another example N_2 is used as a carrier gas. In one embodiment, a carrier gas during an epitaxial deposition process is conducted with neither H_2 nor atomic hydrogen. However, an inert gas is used as a carrier gas, such as N_2, Ar, He and combinations thereof. Carrier gases may be combined in various ratios during some embodiments of the process.

[0018] In one embodiment, a carrier gas includes N_2 and/or Ar to maintain available sites on the silicon compound film. The presence of hydrogen on the silicon compound surface limits the number of available sites (*i.e.,* passivates) for Si or SiGe to grow when an abundance of H_2 is used as a carrier gas. Consequently, a passivated surface limits the growth rate at a given temperature, particularly at lower

temperatures (e.g., <650°C). Therefore, a carrier gas of N_2 and/or Ar may be used during a process at lower temperature and reduce the thermal budget without sacrificing growth rate.

[0019] In one embodiment of the invention, a silicon compound film is epitaxially grown as a Si film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During this deposition technique, silicon precursor (*e.g.,* silane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2) and an etchant (*e.g.,* HCl). The flow rate of the silane is in the range from about 5 sccm to about 500 sccm. The flow rate of the carrier gas is from about 1,000 sccm to about 60,000 sccm. The flow rate of the etchant is from about 5 sccm to about 1,000 sccm. The process chamber is maintained with a pressure from about 0.1 Torr to about 200 Torr, preferably at about 15 Torr. The substrate is kept at a temperature in the range from about 500°C to about 1,000°C, preferably from about 600°C to about 900°C for example, from 600°C to 750°C, for another example from 650°C to 800°C. The mixture of reagents is thermally driven to react and epitaxially deposit crystalline silicon. The HCl etches any deposited amorphous silicon or polycrystalline silicon from dielectric features upon the surface of the substrate. The process is conducted to form the deposited silicon compound with a thickness in a range from about 100 Å to about 3,000 Å and at a deposition rate between about 50 Å/min and about 600 Å/min, preferably at about 150 Å/min. In one embodiment, the silicon compound has a thickness greater than 500 Å, such as about 1,000 Å.

[0020] Etchants are utilized to control the areas on the device to be free of deposited silicon compound. Etchants that are useful during deposition processes of the invention include HCl, HF, HBr, Si_2Cl_6, $SiCl_4$, Cl_2SiH_2, CCl_4, Cl_2 and combinations thereof. Other silicon precursors, besides silane, that are useful while depositing silicon compounds include higher silanes and organosilanes. Higher silanes include the compounds with the empirical formula $Si_xH_{(2x+2)}$, such as disilane (Si_2H_6), trisilane (Si_3H_8) and tetrasilane (Si_4H_{10}), as well as others. Organosilanes include compounds with the empirical formula $R_ySi_xH_{(2x+2-y)}$, where R = methyl, ethyl,

propyl or butyl, such as methylsilane ($(CH_3)SiH_3$), dimethylsilane ($(CH_3)_2SiH_2$), ethylsilane ($(CH_3CH_2)SiH_3$), methyldisilane ($(CH_3)Si_2H_5$), dimethyldisilane ($(CH_3)_2Si_2H_4$) and hexamethyldisilane ($(CH_3)_6Si_2$). Organosilane compounds have been found to be advantageous silicon sources and carbon sources during embodiments of the present invention to incorporate carbon in to deposited silicon compound.

[0021] In another embodiment of the invention, a silicon compound film is epitaxially grown as a SiGe film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During this deposition technique, silicon precursor (*e.g.,* silane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a germanium source (*e.g.,* GeH_4) and an etchant (*e.g.,* HCl). The flow rate of the silane is in the range from about 5 sccm to about 500 sccm. The flow rate of the carrier gas is from about 1,000 sccm to about 60,000 sccm. The flow rate of the germanium source is from about 0.1 sccm to about 10 sccm. The flow rate of the etchant is from about 5 sccm to about 1,000 sccm. The process chamber is maintained with a pressure from about 0.1 Torr to about 200 Torr, preferably at about 15 Torr. The substrate is kept at a temperature in the range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon compound, namely a silicon germanium film. The HCl etches any deposited amorphous SiGe compounds from dielectric features upon the surface of the substrate. The process is conducted to form the deposited SiGe compound with a thickness in a range from about 100 Å to about 3,000 Å and at a deposition rate between about 50 Å/min and about 300 Å/min, preferably at about 150 Å/min. The germanium concentration is in the range from about 1 atomic percent to about 30 atomic percent of the SiGe compound, preferably at about 20 atomic percent.

[0022] Other germanium sources or precursors, besides germane, that are useful while depositing silicon compounds include higher germanes and organogermanes. Higher germanes include the compounds with the empirical formula $Ge_xH_{(2x+2)}$, such

as digermane (Ge_2H_6), trigermane (Ge_3H_8) and tetragermane (Ge_4H_{10}), as well as others. Organogermanes include compounds with the empirical formula $R_yGe_xH_{(2x+2-y)}$, where R = methyl, ethyl, propyl or butyl, such as methylgermane ($(CH_3)GeH_3$), dimethylgermane ($(CH_3)_2GeH_2$), ethylgermane ($(CH_3CH_2)GeH_3$), methyldigermane ($(CH_3)Ge_2H_5$), dimethyldigermane ($(CH_3)_2Ge_2H_4$) and hexamethyldigermane ($(CH_3)_6Ge_2$). Germanes and organogermane compounds have been found to be an advantageous germanium sources and carbon sources during embodiments of the present invention to incorporate germanium and carbon in to the deposited silicon compounds, namely SiGe and SiGeC compounds.

[0023] In one embodiment of the invention, a silicon compound film is epitaxially grown as a doped Si film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During this deposition technique, silicon precursor (*e.g.,* silane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a dopant (*e.g.,* B_2H_6) and an etchant (*e.g.,* HCl). The flow rate of the silane is in the range from about 5 sccm to about 500 sccm. The flow rate of the carrier gas is from about 1,000 sccm to about 60,000 sccm. The flow rate of the dopant is from about 0.01 sccm to about 3 sccm. The flow rate of the etchant is from about 5 sccm to about 1,000 sccm. The process chamber is maintained with a pressure from about 0.1 Torr to about 200 Torr, preferably at about 15 Torr. The substrate is kept at a temperature in the range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The mixture of reagents is thermally driven to react and epitaxially deposit doped silicon films. The HCl etches any deposited amorphous silicon or polycrystalline silicon from dielectric features upon the surface of the substrate. The process is conducted to form the deposited, doped silicon compound with a thickness in a range from about 100 Å to about 3,000 Å and at a deposition rate between about 50 Å/min and about 600 Å/min, preferably at about 150 Å/min.

[0024] Dopants provide the deposited silicon compounds with various conductive characteristics, such as directional electron flow in a controlled and desired pathway required by the electronic device. Films of the silicon compounds are doped with

particular dopants to achieve the desired conductive characteristic. In one embodiment, the silicon compound is doped p-type, such as by using diborane to add boron at a concentration in the range from about 10^{15} atoms/cm^3 to about 10^{21} atoms/cm^3. In one embodiment, the p-type dopant has a concentration of at least 5×10^{19} atoms/cm^3. In another embodiment, the p-type dopant is in the range from about 1×10^{20} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3. In another embodiment, the silicon compound is doped n-type, such as with phosphorus and/or arsenic to a concentration in the range from about 10^{15} atoms/cm^3 to about 10^{21} atoms/cm^3.

[0025] Besides diborane, other boron containing dopants include boranes and organoboranes. Boranes include borane, triborane, tetraborane and pentaborane, while alkylboranes include compounds with the empirical formula $R_xBH_{(3-x)}$, where R = methyl, ethyl, propyl or butyl and x = 0, 1, 2 or 3. Alkylboranes include trimethylborane ($(CH_3)_3B$), dimethylborane ($(CH_3)_2BH$), triethylborane ($(CH_3CH_2)_3B$) and diethylborane ($(CH_3CH_2)_2BH$). Dopants also include arsine (AsH_3), phosphine (PH_3) and alkylphosphines, such as with the empirical formula $R_xPH_{(3-x)}$, where R = methyl, ethyl, propyl or butyl and x = 0, 1, 2 or 3. Alkylphosphines include trimethylphosphine ($(CH_3)_3P$), dimethylphosphine ($(CH_3)_2PH$), triethylphosphine ($(CH_3CH_2)_3P$) and diethylphosphine ($(CH_3CH_2)_2PH$).

[0026] In another embodiment of the invention, a silicon compound film is epitaxially grown to produce a doped SiGe. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During this deposition technique, silicon precursor (*e.g.,* silane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a germanium source (*e.g.,* GeH_4), a dopant (*e.g.,* B_2H_6) and an etchant (*e.g.,* HCl). The flow rate of the silane is in the range from about 5 sccm to about 500 sccm. The flow rate of the carrier gas is from about 1,000 sccm to about 60,000 sccm. The flow rate of the germanium source is from about 0.1 sccm to about 10 sccm. The flow rate of the dopant is from about 0.01 sccm to about 3 sccm. The flow rate of the etchant is from about 5 sccm to about 1,000 sccm. The process chamber is maintained with a pressure from about 0.1 Torr to about 200 Torr, preferably at about 15 Torr. The

substrate is kept at a temperature in the range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon compound, namely a silicon germanium film. The HCl etches any deposited amorphous SiGe from features upon the surface of the substrate. The process is conducted to form the doped SiGe compound with a thickness in a range from about 100 Å to about 3,000 Å and at a rate between about 50 Å/min and about 600 Å/min, preferably at about 150 Å/min. The germanium concentration is in the range from about 1 atomic percent to about 30 atomic percent of the SiGe compound, preferably at about 20 atomic percent. The boron concentration is in the range from about 1×10^{20} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3 of the SiGe compound, preferably at about 2×10^{20} atoms/cm^3.

[0027] In another embodiment of the invention, a silicon compound film is epitaxially grown as a SiGeC film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During this deposition technique, silicon precursor (*e.g.,* silane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a germanium source (*e.g.,* GeH_4), a carbon source (*e.g.,* CH_3SiH_3) and an etchant (*e.g.,* HCl). The flow rate of the silane is in the range from about 5 sccm to about 500 sccm. The flow rate of the carrier gas is from about 1,000 sccm to about 60,000 sccm. The flow rate of the germanium source is from about 0.1 sccm to about 10 sccm. The flow rate of the carbon source is from about 0.1 sccm to about 50 sccm. The flow rate of the etchant is from about 5 sccm to about 1,000 sccm. The process chamber is maintained with a pressure from about 0.1 Torr to about 200 Torr, preferably at about 15 Torr. The substrate is kept at a temperature in the range from about 500°C to about 1,000°C, preferably from about 500°C to about 700°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon compound, namely a silicon germanium carbon film. The HCl etches any deposited amorphous or polycrystalline SiGeC compounds from dielectric features upon the surface of the substrate. The process is conducted to form the deposited SiGeC compound with a

thickness in a range from about 100 Å to about 3,000 Å and at a deposition rate between about 50 Å/min and about 600 Å/min, preferably at about 150 Å/min. The germanium concentration is in the range from about 1 atomic percent to about 30 atomic percent of the SiGeC compound, preferably at about 20 atomic percent. The carbon concentration is in the range from about 0.1 atomic percent to about 5 atomic percent, preferably at about 2 atomic percent of the SiGeC compound.

[0028] Other carbon sources or precursors, besides ethylene or methane, are useful while depositing silicon compounds and include alkyls, alkenes and alkynes of ethyl, propyl and butyl. Such carbon sources include ethyne (C_2H_2), propane (C_3H_8), propene (C_3H_6), butyne (C_4H_6), as well as others. Other carbon sources include organosilane compounds, as described in relation to silicon sources.

[0029] In another embodiment of the invention, a silicon compound film is epitaxially grown as a doped-SiGeC film. A substrate (*e.g.,* 300 mm OD) containing a semiconductor feature is placed into the process chamber. During this deposition technique, silicon precursor (*e.g.,* silane) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a germanium source (*e.g.,* GeH_4), a carbon source (*e.g.,* CH_3SiH_3), a dopant (*e.g.,* B_2H_6) and an etchant (*e.g.,* HCl). The flow rate of the silane is in the range from about 5 sccm to about 500 sccm. The flow rate of the carrier gas is from about 1,000 sccm to about 60,000 sccm. The flow rate of the germanium source is from about 0.1 sccm to about 10 sccm. The flow rate of the carbon source is from about 0.1 sccm to about 50 sccm. The flow rate of the dopant is from about 0.01 sccm to about 3 sccm. The flow rate of the etchant is from about 5 sccm to about 1,000 sccm. The process chamber is maintained with a pressure from about 0.1 Torr to about 200 Torr, preferably at about 15 Torr. The substrate is kept at a temperature in the range from about 500°C to about 1,000°C, preferably from about 500°C to about 700°C. The reagent mixture is thermally driven to react and epitaxially deposit a silicon compound, namely a doped silicon germanium carbon film. The HCl etches any deposited amorphous or polycrystalline SiGeC compounds from dielectric features upon the surface of the substrate. The process is conducted to form the deposited SiGeC compound with a

thickness in a range from about 100 Å to about 3,000 Å and at a deposition rate between about 50 Å/min and about 600 Å/min, preferably at about 150 Å/min. The germanium concentration is in the range from about 1 atomic percent to about 30 atomic percent of the SiGeC compound, preferably at about 20 atomic percent. The carbon concentration is in the range from about 0.1 atomic percent to about 5 atomic percent of the SiGeC compound, preferably at about 2 atomic percent. The boron concentration is in the range from about 1×10^{20} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3 of the SiGe compound, preferably at about 2×10^{20} atoms/cm^3.

[0030] In another embodiment of the invention, a second silicon compound film is epitaxially grown as a SiGe film by using dichlorosilane, subsequently to depositing any of the silicon compounds as described above via silane as a silicon source. A substrate (*e.g.,* 300 mm OD) containing any of the above described silicon containing compounds is placed into the process chamber. During this deposition technique, silicon precursor (*e.g.,* Cl_2SiH_2) is flown concurrently into the process chamber with a carrier gas (*e.g.,* H_2 and/or N_2), a germanium source (*e.g.,* GeH_4) and an etchant (*e.g.,* HCl). The flow rate of the dichlorosilane is in the range from about 5 sccm to about 500 sccm. The flow rate of the carrier gas is from about 1,000 sccm to about 60,000 sccm. The flow rate of the germanium source is from about 0.1 sccm to about 10 sccm. The flow rate of the etchant is from about 5 sccm to about 1,000 sccm. The process chamber is maintained with a pressure from about 0.1 Torr to about 200 Torr, preferably at about 15 Torr. The substrate is kept at a temperature in the range from about 500°C to about 1,000°C, preferably from about 700°C to about 900°C. The reagent mixture is thermally driven to react and epitaxially deposit a second silicon compound, namely a silicon germanium film. The HCl etches any deposited amorphous or polycrystalline SiGe compounds from any dielectric features upon the surface of the substrate. The process is conducted to form the deposited SiGe compound with a thickness in a range from about 100 Å to about 3,000 Å and at a deposition rate between about 10 Å/min and about 100 Å/min, preferably at about 50 Å/min. The germanium concentration is in the range from about 1 atomic percent to about 30 atomic percent of the SiGe compound,

preferably at about 20 atomic percent. This embodiment describes a process to deposit a SiGe film, though substitution of silane with dichlorosilane to any of the previously described embodiments will produce a second silicon containing film. In another embodiment, a third silicon containing layer is deposited using any of the silane based process discussed above.

[0031] Therefore, in one embodiment, a silicon compound laminate film may be deposited in sequential layers of silicon compound by altering the silicon precursor between silane and dichlorosilane. In one example, a laminate film of about 2,000 Å is formed by depositing four silicon compound layers (each of about 500 Å), such that the first and third layers are deposited using dichlorosilane and the second and fourth layers are deposited using silane. In another aspect of a laminate film, the first and third layers are deposited using silane and the second and fourth layers are deposited using dichlorosilane. The thickness of each layer is independent from each other; therefore, a laminate film may have various thicknesses of the silicon compound layers.

[0032] In one embodiment, dichlorosilane is used to deposit the silicon compound layer when the previous layer contains surface islands (*e.g.*, contamination or irregularity to film). A process incorporating dichlorosilane may be less sensitive to the surface islands while depositing the silicon compound layer over the previous layer. The use of dichlorosilane as the silicon source has a high horizontal or lateral growth rate relative to the use of silane. Once the surface island is covered and the silicon compound layer has a consistent surface, dichlorosilane is replaced with silane and deposition of the silicon compound layer is continued.

[0033] Embodiments of the invention teach processes to deposit silicon compounds on many substrates and surfaces. Substrates on which embodiments of the invention may be useful include, but are not limited to semiconductor wafers, such as crystalline silicon (*e.g.*, Si<100> and Si<111>), silicon oxide, silicon germanium, doped or undoped wafers and patterned or non-patterned wafers. Substrates have a variety of geometries (*e.g.*, round, square and rectangular) and

sizes (*e.g.,* 200 mm OD, 300 mm OD). Surfaces and./or substrates include wafers, films, layers and materials with dielectric, conductive and barrier properties and include polysilicon, silicon on insulators (SOI), strained and unstrained lattices. Pretreatment of surfaces includes polishing, etching, reduction, oxidation, hydroxylation, annealing and baking. In one embodiment, wafers are dipped into a 1% HF solution, dried and baked in a hydrogen atmosphere at 800°C.

[0034] In one embodiment, silicon compounds include a germanium concentration within the range from about 0 atomic percent to about 95 atomic percent. In another embodiment, a germanium concentration is within the range from about 1 atomic percent to about 30 atomic percent, preferably from about 15 atomic percent to about 25 atomic percent and more preferably at about 20 atomic percent. Silicon compounds also include a carbon concentration within the range from about 0 atomic percent to about 5 atomic percent. In other aspects, a carbon concentration is within the range from about 200 ppm to about 2 atomic percent.

[0035] The silicon compound films of germanium and/or carbon are produced by various processes of the invention and can have consistent, sporadic or graded elemental concentrations. Graded silicon germanium films are disclosed in U.S. Patent Applications 20020174826 and 20020174827 assigned to Applied Material, Inc., and are incorporated herein by reference in entirety for the purpose of describing methods of depositing graded silicon compound films. In one embodiment, silane and a germanium source (*e.g.,* GeH_4) are used to deposit silicon germanium containing films. In this embodiment, the ratio of silane and germanium source can be varied in order to provide control of the elemental concentrations while growing graded films. In another embodiment, silane and a carbon source (*e.g.,* CH_3SiH_3) are used to deposit silicon carbon containing films. The ratio of silane and carbon source can be varied in order to provide control of the elemental concentration while growing homogenous or graded films. In another embodiment, silane, a germanium source (*e.g.,* GeH_4) and a carbon source (*e.g.,* CH_3SiH_3) are used to deposit silicon germanium carbon containing films. The ratio

of silane, germanium and carbon source can be varied in order to provide control of the elemental concentration while growing homogenous or graded films.

[0036] In processes of the invention, silicon compound films are grown by chemical vapor deposition (CVD) processes, wherein CVD processes include atomic layer deposition (ALD) processes and/or atomic layer epitaxy (ALE) processes. Chemical vapor deposition includes the use of many techniques, such as plasma-assisted CVD (PA-CVD), atomic layer CVD (ALCVD), organometallic or metalorganic CVD (OMCVD or MOCVD), laser-assisted CVD (LA-CVD), ultraviolet CVD (UV-CVD), hot-wire (HWCVD), reduced-pressure CVD (RP-CVD), ultra-high vacuum CVD (UHV-CVD) and others. In one embodiment, the preferred process of the present invention is to use thermal CVD to epitaxially grow or deposit the silicon compound, whereas the silicon compound includes silicon, SiGe, SiC, SiGeC, doped variants thereof and combinations thereof.

[0037] The processes of the invention can be carried out in equipment known in the art of ALE, CVD and ALD. The apparatus brings the sources into contact with a heated substrate on which the silicon compound films are grown. The processes can operate at a range of pressures from about 1 mTorr to about 2,300 Torr, preferably between about 0.1 Torr and about 200 Torr. Hardware that can be used to deposit silicon-containing films includes the Epi Centura® system and the Poly Gen® system available from Applied Materials, Inc., located in Santa Clara, California. An ALD apparatus is disclosed in U.S. Patent Application 20030079686, assigned to Applied Material, Inc., and entitled "Gas Delivery Apparatus and Methods for ALD", and is incorporated herein by reference in entirety for the purpose of describing the apparatus. Other apparatuses include batch, high-temperature furnaces, as known in the art.

[0038] The processes are extremely useful while depositing silicon compound layers in Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) and bipolar transistors as depicted in Figures 1A-1C. Herein, silicon compounds are the deposited layers or films and include Si, SiGe, SiC, SiGeC, doped variants thereof

and combinations thereof, epitaxially grown during the processes of the present invention. The silicon compounds include strained or unstrained layers within the films.

[0039] Figures 1A-1B show the epitaxially grown silicon compound on a MOSFET. The silicon compound is deposited to the source/drain features of the device. The silicon compound adheres and grows from the crystal lattice of the underlying layer and maintains this arrangement as the silicon compound grows with thickness. In one embodiment, Figure 1A demonstrates the silicon compound deposited as a source/drain extension source, while in another embodiment, Figure 1B shows the silicon compound deposited as an elevated source/drain (ESD).

[0040] The source/drain layer 12 is formed by ion implantation of the substrate 10. Generally, the substrate 10 is doped n-type while the source/drain layer 12 is doped p-type. Silicon compound layer 14 is epitaxially grown to the source/drain layer 12 by the various embodiments of the present invention. A gate oxide layer 18 bridges the either the segmented silicon compound layer 14 (Figure 1A) or the segmented source/drain layer 12 (Figure 1B). Generally, gate oxide layer 18 is composed of silicon dioxide, silicon oxynitride or tantalum oxide. Partially encompassing the gate oxide layer 18 is a spacer 16, which is usually an isolation material such as a nitride/oxide stack (*e.g.*, $Si_3N_4/SiO_2/Si_3N_4$). Also within the spacer 16 is off-set layers 20 (*e.g.*, Si_3N_4) and the gate layer 22 (*e.g.*, W or Ni).

[0041] In another embodiment, Figure 1C depicts the deposited silicon compound layer 34 as a base layer of a bipolar transistor. The silicon compound layer 34 is epitaxially grown with the various embodiments of the invention. The silicon compound layer 34 is deposited to an n-type collector layer 32 previously deposited to substrate 30. The transistor further includes isolation layer 33 (*e.g.*, SiO_2 or Si_3N_4), contact layer 36 (*e.g.*, heavily doped poly-Si), off-set layer 38 (*e.g.*, Si_3N_4) and a second isolation layer 40 (*e.g.*, SiO_2 or Si_3N_4).

[0042] In one embodiment, as depicted in Figures 2A-2F, a source/drain extension is formed within a MOSFET wherein the silicon compound layers are

epitaxially and selectively deposited on the surface of the substrate. Figure 2A depicts a source/drain layer 132 formed by implanting ions into the surface of a substrate 130. The segments of source/drain layer 132 are bridged by the gate 136 formed within off-set layer 134. A portion of the source/drain layer is etched and wet-cleaned, to produce a recess 138, as in Figure 2B.

[0043] Figure 2C illustrates several embodiments of the present invention, in which silicon compound layers 140 (epitaxial) and 142 (polycrystalline) are selectively deposited. Silicon compound layers 140 and 142 are deposited simultaneously without depositing on the off-set layer 134. Silicon compound layers 140 and 142 are generally doped SiGe containing layers with a germanium concentration at about 1 atomic percent to about 30 atomic percent, preferably at about 20 atomic percent and a dopant (*e.g.,* B, As or P) concentration from about 1×10^{20} atoms/cm^3 to about 2.5×10^{21} atoms/cm^3, preferably at about 2×10^{20} atoms/cm^3. During the next step, Figure 2D shows the nitride spacer 144 (*e.g.,* Si_3N_4) deposited to the off-set layer 134.

[0044] Figure 2E depicts another embodiment of the present invention, in which a silicon compound is epitaxially and selectively deposited as silicon compound layer 148. Silicon compound layer 148 is deposited on layer 140 (doped-SiGe). Polysilicon layer 146 is deposited on the silicon compound layer 142 (doped-SiGe).

[0045] In the next step shown in Figure 2F, a metal layer 154 is deposited over the features and the device is annealed. The metal layer 154 includes cobalt, nickel or titanium, among other metals. During the annealing process, polysilicon layer 146 and silicon compound layer 148 are converted to metal silicide layers, 150 and 152, respectively. That is, when cobalt is deposited as metal layer 154, then metal silicide layers 150 and 152 are cobalt silicide.

[0046] The silicon compound is heavily doped with the *in-situ* dopants. Therefore, annealing steps of the prior art are omitted and the overall throughput is shorter. An increase of carrier mobility along the channel and subsequent drive current is achieved with the optional addition of germanium and/or carbon into the

silicon compound layer. Selectively grown epilayers of the silicon compound above the gate oxide level can compensate junction consumption during the silicidation, which can relieve concerns of high series resistance of ultra shallow junctions. These two applications can be implemented together as well as solely for CMOS device fabrication.

[0047] Silicon compounds are utilized within embodiments of the processes to deposit silicon compounds films used for Bipolar (*e.g.,* base, emitter, collector, emitter contact), BiCMOS (*e.g.,* base, emitter, collector, emitter contact) and CMOS (*e.g.,* channel, source/drain, source/drain extension, elevated source/drain, substrate, strained silicon, silicon on insulator and contact plug). Other embodiments of processes teach the growth of silicon compounds films that can be used as gate, base contact, collector contact, emitter contact, elevated source/drain and other uses.

[0048] Example 1: Boron doped silicon germanium deposition: A substrate, Si<100>, (*e.g.,* 300 mm OD) was employed to investigate selective, monocrystalline film growth by CVD. A dielectric feature existed on the surface of the wafer. The wafer was prepared by subjecting to a 1% HF dip for 45 seconds. The wafer was loaded into the deposition chamber (Epi Centura® chamber) and baked in a hydrogen atmosphere at 800°C for 60 seconds to remove native oxide. A flow of carrier gas, hydrogen, was directed towards the substrate and the source compounds were added to the carrier flow. Silane (100 sccm) and germane (6 sccm) were added to the chamber at 15 Torr and 725°C. Hydrogen chloride was delivered with a flow rate of 460 sccm. Diborane was delivered with a flow rate of 1 sccm. The substrate was maintained at 725°C. Deposition was carried out for 5 minutes to form a 500 Å SiGe film with a germanium concentration of 21 atomic percent and the boron concentration was 2.0×10^{20} cm^{-3}.

[0049] Example 2: Phosphorus doped silicon germanium deposition: A substrate was prepared as in Example 1. The wafer was loaded into the deposition chamber (Epi Centura® chamber) and baked in a hydrogen atmosphere at 800°C for 60

seconds to remove native oxide. A flow of carrier gas, hydrogen, was directed towards the substrate and the source compounds were added to the carrier flow. Silane (100 sccm) and germane (4 sccm) were added to the chamber at 15 Torr and 725°C. Hydrogen chloride was delivered with a flow rate of 250 sccm. Phosphine was delivered to the chamber with a flow rate of 1 sccm. The substrate was maintained at 725°C. Deposition was carried out for 5 minutes to form a 500 Å SiGe film with a germanium concentration of 20 atomic percent and the phosphorus concentration was 1.6×10^{20} cm^{-3}.

[0050] Example 3: Boron doped silicon germanium deposition with sequential Cl_2SiH_2 and SiH_4 flows: The substrates were prepared as in Example 1. The wafer was loaded into the deposition chamber (Epi Centura® chamber) and baked in a hydrogen atmosphere at 800°C for 60 seconds to remove native oxide. A flow of carrier gas, hydrogen, was directed towards the substrate and the source compounds were added to the carrier flow. Dichlorosilane (100 sccm), germane (2.8 sccm), and diborane (0.3 sccm) were added to the chamber at 15 Torr and 725°C. Hydrogen chloride was delivered with a flow rate of 190 sccm. The substrate was maintained at 725°C. Deposition was conducted for 72 seconds to form a first layer of silicon compound with a thickness of 50 Å. On top of the first layer, a subsequent epitaxial layer (*i.e.*, a second layer of silicon compound) was deposited using silane (100 sccm), germane (6 sccm), hydrogen chloride (460 sccm) and diborane (1 sccm). The chamber pressure and temperature remained constant (15 Torr and 725°C) and the deposition was conducted for 144 seconds to form 250 Å layer of the second layer.

[0051] Examples 4: Boron doped silicon germanium deposition with sequential using SiH_4 and Cl_2SiH_2: The substrates were prepared as in Example 1. The wafer was loaded into the deposition chamber (Epi Centura® chamber) and baked in a hydrogen atmosphere at 800°C for 60 seconds to remove native oxide. A flow of carrier gas, hydrogen, was directed towards the substrate and the source compounds were added to the carrier flow. Silane (100 sccm), germane (6 sccm),

and diborane (1 sccm) were added to the chamber at 15 Torr and 725°C. Hydrogen chloride was delivered with a flow rate of 460 sccm. The substrate was maintained at 725°C. Deposition was conducted for 144 seconds to form a first layer of silicon compound with a thickness of 250 Å. On top of the first layer, a second layer of silicon compound was sequentially deposited using dichlorosilane (100 sccm), germane (2.8 sccm), hydrogen chloride (190 sccm) and diborane (0.3 sccm). The chamber pressure and temperature remained constant (15 Torr and 725°C) was conducted for 72 seconds to form additional 50 Å layer.

[0052] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.